CONTINUOUS INTERNAL EVALUATION- 3

Dept:EC	Sem / Div:III A&B	Sub:Digital System Design	S Code:18EC34
Date:16-2-2021	Time: 2:30-4:00 pm	Max Marks: 50	Elective:N
Note: Answer any 2 full questions, choosing one full question from each part.			

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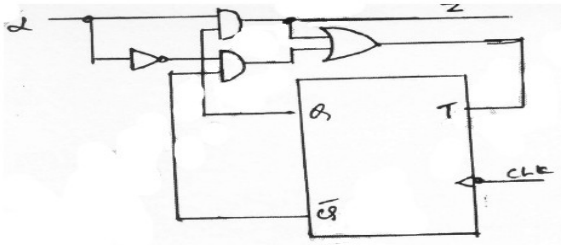
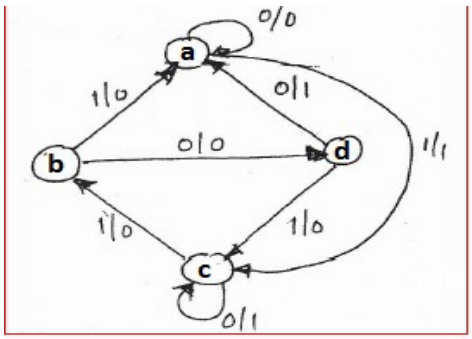
QN		Questions	Marks	RBT	COs
		PART A			
1	a	Design mod-6 counter using D-flipflop. The sequence is 000, 001, 011, 100, 101, 111,..000.	10	L3	CO3
	b	Analyze the following sequential circuit. Construct transition table, state table and state diagram. 	10	L3	CO3
	c	Explain State machine Notations.	5	L2	CO3
		OR			
2	a	Design mod-5 counter using T-Flipflop and implement it.	10	L3	CO3
	b	Construct the state diagram for Excess-3 to BCD code converter.	10	L3	CO4
	c	Explain with block diagram Serial Adder with accumulator	5	L2	CO3
		PART B			
3	a	A sequential network has one input and one output the state diagram is shown below. Design the sequential circuit using T-flipflop. 	10	L3	CO4
	b	Construct a Mealy state diagram that will detect input secuence 10110, when input pattern is detected Z is asserted high. Design using D-Flipflop	15	L3	CO4
		OR			
4	a	Explain Melay and Moore models with example.	8	L2	CO3
	b	Design a iterative circuit which compares two n-bit binary numbers and determines if they are equal or which one is larger if they are not equal.	10	L3	CO4
	c	Write the guidelines for construction of state graphs.	7	L2	CO4

Prepared by: Nisha G R HOD